CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-8 (canceled).

9 (currently amended). The device according to claim 10 ~~8~~, wherein said arithmetic unit checks, in a second comparison process, whether more than a given number of the first fault addresses of one of ~~said~~ the bit lines and ~~said~~ the word lines is stored for one of a word line and a bit line, said arithmetic unit storing, as a new further second fault address, an address of the one of the word line and the bit line for which more than the given number of first fault addresses are stored and taking the new further second fault address into account in subsequent first comparison processes.

10 (currently amended). ~~The device according to claim 8, wherein:~~ A device for reducing a number of addresses of faulty memory cells in a memory cell array having word lines, bit lines and memory cells with respective addresses, the device comprising:

an arithmetic unit;

said arithmetic unit processing, as first fault addresses, the addresses of given ones of the memory cells having been detected as faulty in a test;

said arithmetic unit comparing the first fault addresses with second fault addresses in a first comparison process, the second fault addresses constituting addresses of given ones of the word lines and the bit lines which are to be completely repaired;

said arithmetic unit not storing a respective one of the first fault addresses, if the respective one of the first fault addresses corresponds to a respective one of the second fault addresses, and said arithmetic unit storing the respective one of the first fault addresses, if the respective one of the first fault addresses does not correspond to the respective one of the second fault addresses;

said arithmetic unit ~~has~~ having a first comparison unit, said first comparison unit ~~has~~ having a first row of serially connected registers and a second row of serially connected

registers, each of said registers in said first row is assigned to a respective one of said registers in said second row;

said first comparison unit ~~has~~ having a clock input for receiving a clock signal;

a first one of said registers in said first row is configured to be supplied with a first fault address, said first row of serially connected registers is configured such that the first fault address is shifted forward by a respective one of said registers in said first row at each clock signal; ~~and~~

said first comparison unit comparing, between clock signals, in each case the addresses of assigned ones of said registers of said first row and said second row and deleting an address of one of said registers of said first row, if the addresses of said assigned ones of said registers of said first row and said second row correspond;

said arithmetic unit having a second comparison unit, said second comparison unit having a third row of serially connected registers and a fourth row of serially connected registers, each of said registers in said third row is

assigned to a respective one of said registers in said fourth row;

said second comparison unit having a clock input for receiving the clock signal;

a first one of said registers in said fourth row is configured to be supplied with the first fault address after the clock signal;

said fourth row of serially connected registers is configured such that the first fault address is shifted forward by a respective one of said registers in said third row at each clock signal;

said second comparison unit comparing, between clock signals, in each case the addresses of assigned ones of said registers of said third row and said fourth row and deleting an address of one of said registers of said fourth row, if the addresses of said assigned ones of said registers of said third row and said fourth row correspond;

said second comparison unit reading an address of one of said registers of said fourth row into an assigned one of said registers of said third row if said assigned one of said

registers of said third row is detected as being empty during a comparison;

said second comparison unit serially reading into said first row and processing, in a given operation, the first fault addresses of at least one of a word line and a bit line, said second comparison unit checking, after performing the given operation, whether more than a given number of said serially connected registers of said third row is occupied; and

said arithmetic unit writing an address of one of a checked one of the word lines and a checked one of the bit lines into a free one of said serially connected registers of said second row as a further new second fault address.

11 (canceled).